



Outline

Date: May 31, 2006
Re: Die Retest Project
To: Memo Log
Author: Ken Freed
File#: KXF-
Category:

CC: <Distributed Electronically>

- Outline
- Executive Summary
- Enhancements & Bugs Fixes
- Are the Maps Still Good?
- Spec Updates
- Scheduling Status
- Release Schedule
- Approvals



Executive Summary

What this is:

A revision of the VT2100-KLA1007 prober die retest software to work with EG4080 probers.
A set of follow-on enhancements & minor bug fixes common to VT-KLA and VT-EG Die Retest Software

Die Retest Progression:

- Feb 7, 2006: VT-KLA Die Retest Software was approved for production in PCR4.
 - PCR4 documented in memo KXF-158
 - The 20 VT-KLA tools were retrofitted the following week.
- April 9, 2006: VT-KLA Die Retest Software upgrades installed
- This release is for VT-EG probers
 - Planning and schedule are documented in memo KXF-162 ("CTI Automation Project Prioritization & Planning 15Mar06")

Purpose of this Meeting:

To get approval for soft turn-on, i.e.,

- to run the updated die retest software on rsc'd wafers among seven VT2100-EG4080 testers.

Enhancements & Bug Fixes

These are changes to the VT-KLA prober code base have been incorporated into the VT-EG s/w. We will install them on VT-KLA probers after they are running in production on the VT-EGs

- following correlation experiments/maps and a PCR for the VT-KLAs.

DPRC.EXE Changes:

- DPRC.EXE transfers files between tool and server, and interfaces to the user. The same dprc.exe program runs on both VT-KLA and VT-EG testers
- The 06Apr06 DPRC.EXE release has been running in production on 20 VT-KLA testers since April 19, 2006

```

/* 06Apr06 KXF          New release - lots of changes                               */
/* 21Apr06 KXF  lotmenu.c  Fix indexing problem if less than a whole (scrolled) page of planfiles */
/* 24Apr06 KXF  summary.c  Change printf's to print_and_log_msg in CreateMosproSummary          */
/*                               lotmenu.c  Fix bug if less than one scroll screen worth of wafers to recover */
/*                               waflist.c                                     */
/* 25Apr06 KXF  summary.c  put_red_popup if we are aborting wafer map processing                */
/*                               reload.c                                     */
/* 26Apr06 KXF  nmalloc.c  Convert more put_red_popup calls to print_and_log_msg                */
/*                               summary.c  CreateMosproSummary make planfile name all small letters */
/*                               lotmenu.c  get_user_input - vary prompt width to allow more input without */
/*                               overrunning screen.  Need for longer plan path entry                */
/*                               mospro.c   Longer plan path entry                                */
/* 23May06 KXF  lotmenu.c  Substitute manually edited probe card id info into mospro file if          */
/*                               summary.c  probe card id is not automatically read                */

```

Engineering enhancements in bold

RDPIO.EXE & EGIO.EXE Common Changes

- RDPIO.EXE interfaces to the KLA 1007 probers
- EGIO.EXE interfaces to the EG 4080 probers

The 18Apr06 RDPIO.EXE release has been running in production on 20 VT-KLA testers since April 19, 2006. Changes since then (which have been incorporated into EGIO.EXE) have been:

```
/* 11Apr06 KXF          New release - lots of changes                */
/* 18Apr06 KXF main.c   put sort flow char into the logfile name    */
/*                    rdpio.c                                       */
/* 21Apr06 KXF scrnio.c Revise get_user_choice6 to handle from 2 to 6 choices */
/*                    scrnio.h   Put a 3 choice selection in serio.c::CheckWaferSites, rather */
/*                    serio.c     than a put_foreground_popup and hardcoded choice          */
/* 26Apr06 KXF rdpio.c   Dont exit program if LoadSetupFromDisk fails      */
/* 28Apr06 KXF retest.c New global retest limits RE_TEST_LIMIT <no_of_retests> <percent>*/
/* 12May06 KXF rdpio.c   Call isWafermap_displayed before updating top of map with      */
/*                    DPRC Process Summary message.                          */
/*                    serio.c     Eliminate string_toupper subroutine, since not used.    */
/*                    Using strlwr in the logic instead                       */
```

Engineering enhancements in bold

Are the Maps (coming from the VT-EG testers) Good? - Yes

Ran several - six wafer correlations:

- 1) 8C21001AT - Lot 2611369 Wafers 1 through 6 on VT18 under new software, then ran the same wafers on the same tool under old software

Wafer	Total Sites	Total Shift	%Shift
2611369-01	2692	102	3.79%
2611369-02	2692	73	2.71%
2611369-03	2692	30	1.11%
2611369-04	2692	39	1.45%
2611369-05	2692	109	4.05%
2611369-06	2692	141	5.24%

Retests:

Ran on VT18 (EG Quad Prober) under new software (with retest of bin 10s),
 then ran the same wafers on the same tool under old software (without retest)

Wafer	% Shift	Total Retests	No of Bincode Changes upon Retesting	Bin Code Change Breakdown no of changes: bincode->bincode
2611369-01	3.79%	41	41	40: 10->1 1: 10->8 1: 12->1
2611369-02	2.71%	0		
2611369-03	1.11%	0		
2611369-04	1.45%	0		
2611369-05	4.05%	0		
2611369-06	5.24%	0		



2611369-01

Total Sites	2692
Total Shift	102
% shift	3.79%

Change	Total	% shift
1 to C	37	1.37%
to 1	27	1.00%
8 to 1	10	0.37%
1 to .	7	0.26%
1 to 8	5	0.19%
C to 1	3	0.11%
. to	2	0.07%
1 to .	2	0.07%
1 to 7	2	0.07%
to .	1	0.04%
to 7	1	0.04%
to D	1	0.04%
1 to D	1	0.04%
7 to	1	0.04%
8 to 7	1	0.04%
8 to D	1	0.04%

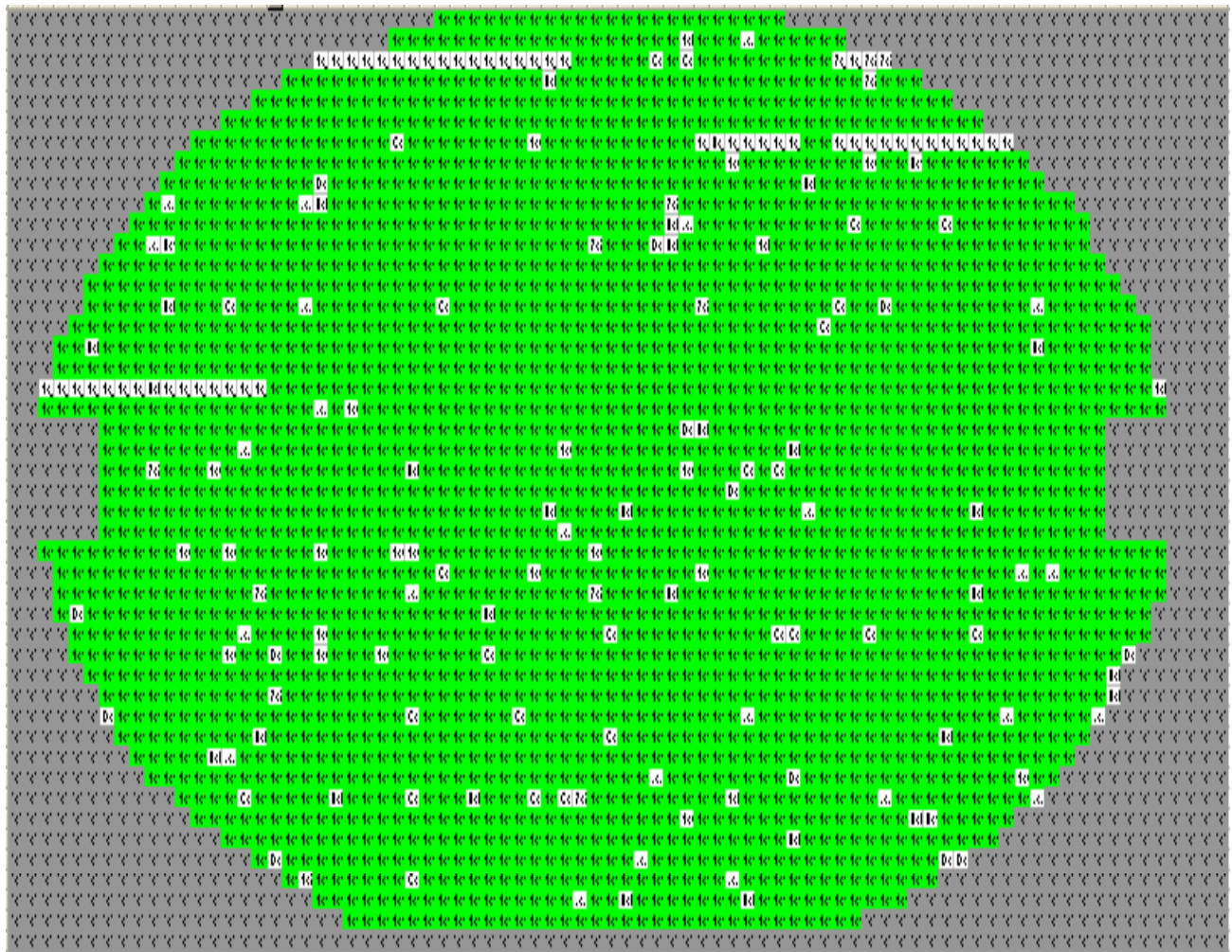
Change	Total	% shift
1 to C	37	1.37%
to 1	27	1.00%
8 to 1	10	0.37%
1 to .	7	0.26%
1 to 8	5	0.19%
C to 1	3	0.11%
. to	2	0.07%
1 to .	2	0.07%
1 to 7	2	0.07%
to .	1	0.04%
to 7	1	0.04%
to D	1	0.04%
1 to D	1	0.04%
7 to	1	0.04%
8 to 7	1	0.04%
8 to D	1	0.04%



Total Sites	2692
Total Shift	109
% Shift	4.05%

2611369-05

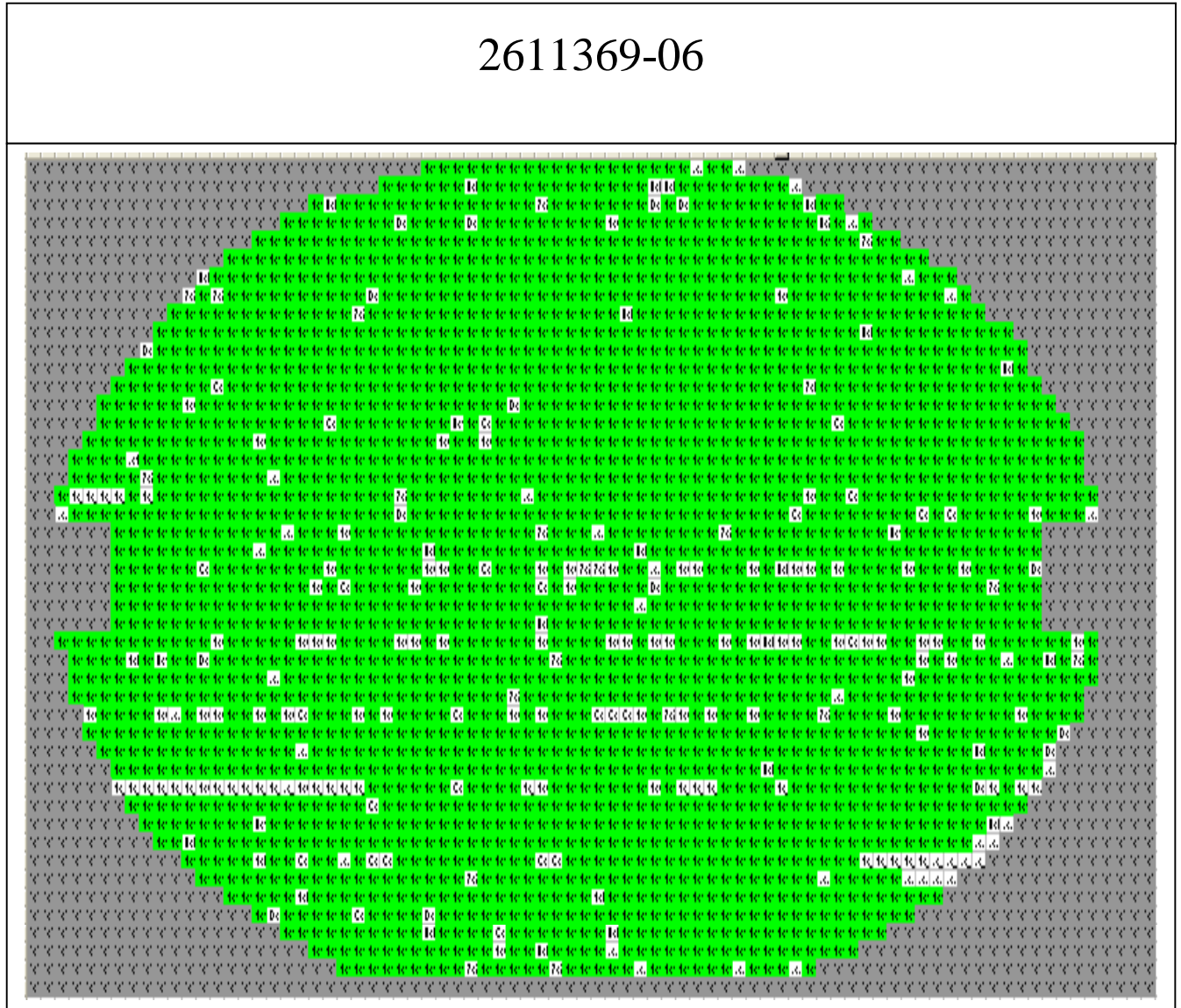
Change	Total	% Shift
1_to__	50	1.86%
C_to_1	26	0.97%
1_to_C	21	0.78%
1_to_8	3	0.11%
8_to_1	3	0.11%
1_to_7	1	0.04%
1_to_D	1	0.04%
7_to__	1	0.04%
8_to__	1	0.04%
8_to_D	1	0.04%
D_to_7	1	0.04%



Total sites	2692
Total shift	141
% shift	5.24%

2611369-06

Change	Total	% shift
1 to C	74	2.75%
1 to	32	1.19%
C to 1	17	0.63%
. to	5	0.19%
8 to 1	4	0.15%
1 to 8	3	0.11%
. to 1	1	0.04%
1 to D	1	0.04%
7 to D	1	0.04%
8 to 7	1	0.04%
D to 8	1	0.04%





2) 8C21001AT - Lot 2611420 Wafers 1 through 6 on VT30 (VT-EG quad with retest of bin 10s), then ran the same lot on VT08 (VT-KLA quad with existing die retest s/w retesting bin 10s)

Wafer	Total Sites	Total Shift	%Shift	Notes
2611420-01	2692	35	1.30%	
2611420-02	2692	29	1.08%	
2611420-03	2692	270	10.03%	poorly yielding wafer
2611420-04	2692	268	9.96%	bin 8 striping problems
2611420-05	2692	68	2.53%	
2611420-06	2692	63	2.34%	



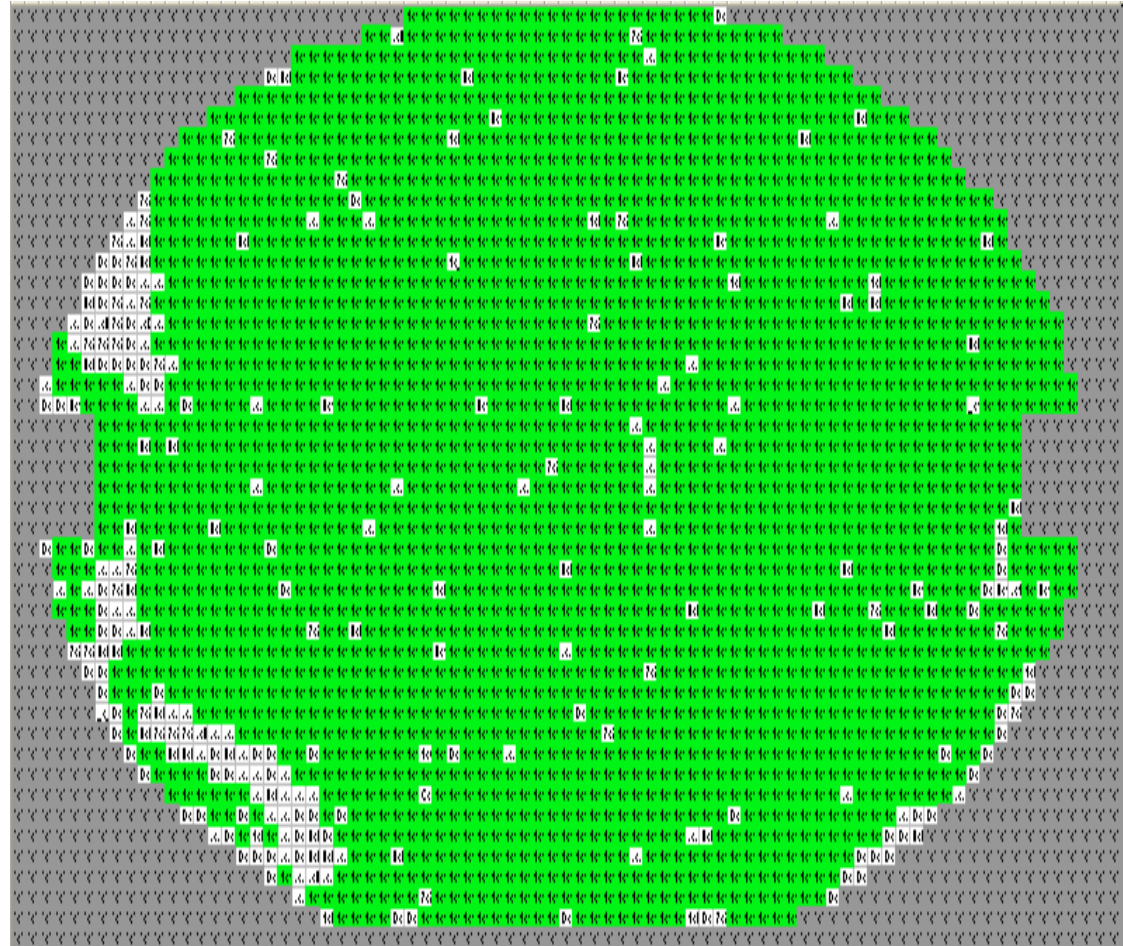
Retests of Bin 10s on Quad Probers:

Wafer	% Shift	VT-EG (new s/w on VT30)			VT-KLA (existing s/w on VT8)		
		Total Retests	No of Bincodes Changes upon Retesting	Bin Code Change Breakdown	Total Retests	No of Bincodes Changes upon Retesting	Bin Code Change Breakdown
2611420-01	1.30%	5	4	4: 10->1	1	0	
2611420-02	1.08%	0			0	0	
2611420-03	10.03%	39	41	14: 10->1 22: 10->7 5: 12->1	0	0	
2611420-04	9.96%	103	98	88: 10->1 5: 10->8 3: 8->1 1: 12->1 1: 10->7	4	4	4: 10->1
2611420-05	2.53%	80	74	70: 10->1 2: 10->7 2: 10->8	10	9	9: 10->1
2611420-06	2.34%	89	88	1: 13->8 80: 10->1 4: 10->7 2: 10->8 1: 8->1	4	2	2: 10->1

2611420-01

Total Sites	2692
Total Shift	35
% Shift	1.30%

Change	Total	% Shift
8 to 1	10	0.37%
1 to 8	6	0.22%
. to 8	4	0.15%
1 to D	4	0.15%
D to .	2	0.07%
D to 8	2	0.07%
. to 1	1	0.04%
. to D	1	0.04%
to 1	1	0.04%
1 to C	1	0.04%
C to 1	1	0.04%
D to 7	1	0.04%

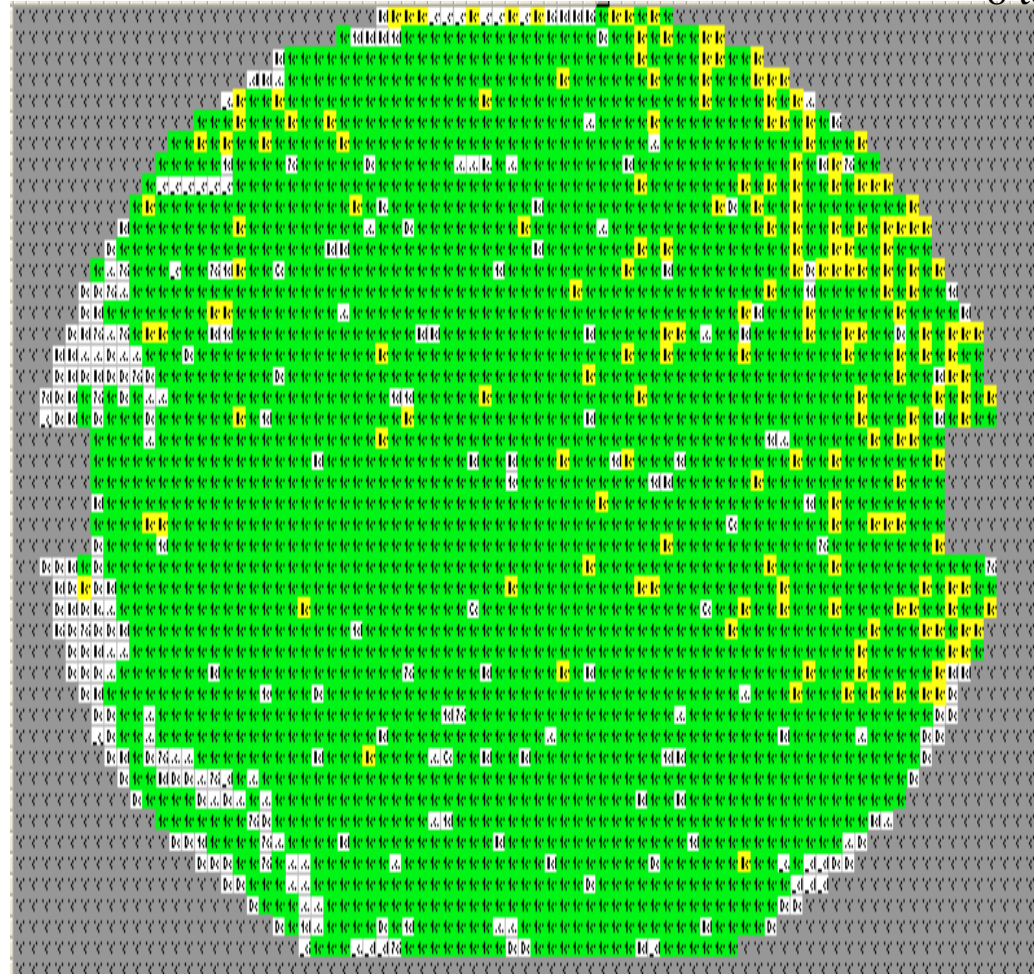


2611420-04

Color Code
Yellow
8 to 1

Total sites	2692
Total Shift	268
% shift	9.96%

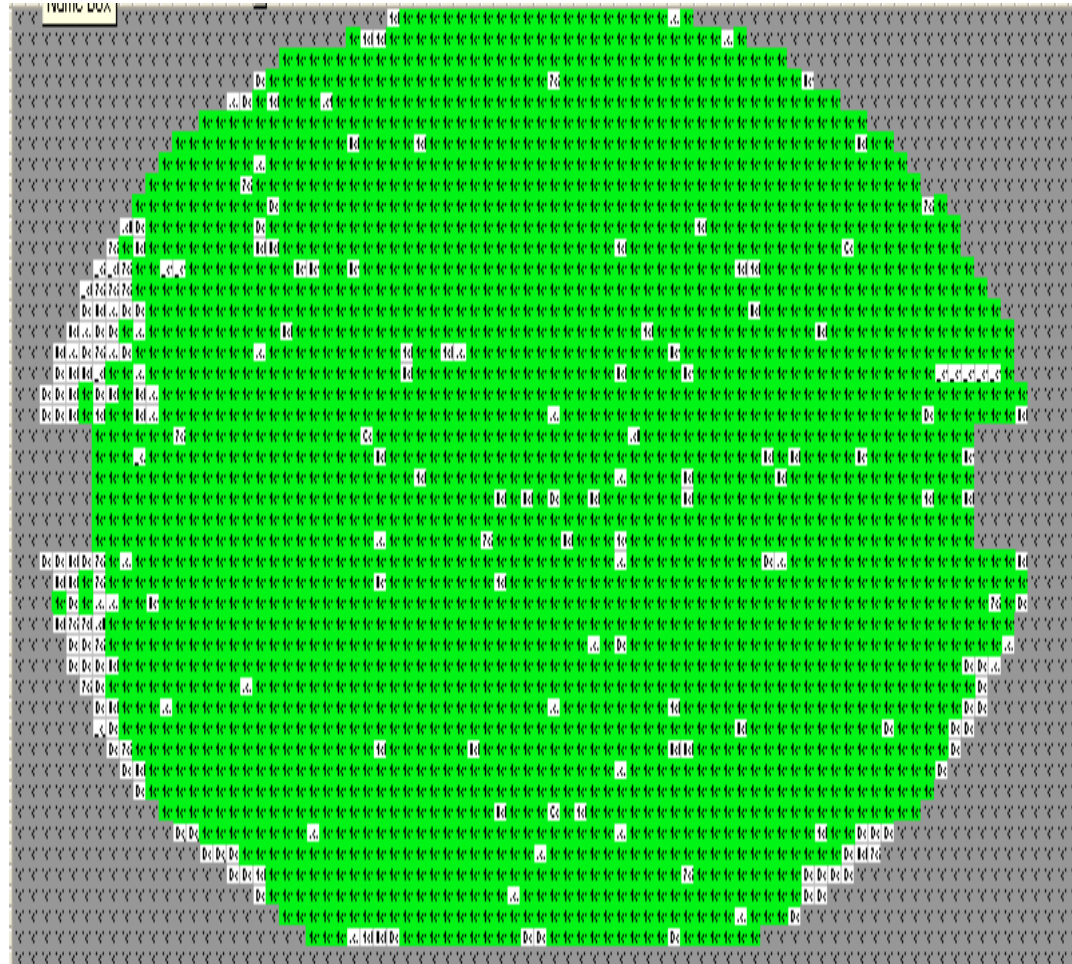
Change	Total	% shift
8_to_1	188	6.98%
1_to_8	22	0.82%
_to_1	13	0.48%
_to_D	9	0.33%
8_to_D	9	0.33%
C_to_1	5	0.19%
8_to_7	4	0.15%
to.	3	0.11%
1_to_D	3	0.11%
8_to_.	3	0.11%
1_to_C	2	0.07%
D_to_1	2	0.07%
D_to_7	2	0.07%
._to_8	1	0.04%
_to_7	1	0.04%
7_to_D	1	0.04%



2611420-06

Total sites	2692
Total shift	63
% shift	2.34%

Change	Total	% shift
1 to 8	21	0.78%
8 to 1	10	0.37%
to 1	7	0.26%
to 8	3	0.11%
to D	3	0.11%
C to 1	3	0.11%
D to	3	0.11%
D to 7	3	0.11%
D to 8	2	0.07%
to 1	1	0.04%
to	1	0.04%
to 7	1	0.04%
1 to C	1	0.04%
1 to D	1	0.04%
7 to 8	1	0.04%
8 to D	1	0.04%
D to	1	0.04%



The image shows a large grid of data points, likely a test results table. The grid is composed of many rows and columns of small text. Some cells are highlighted in green, and some are highlighted in red, indicating specific test results or shifts. The text in the grid is mostly small and difficult to read, but it appears to be a list of test sites and their corresponding results.

Spec Updates

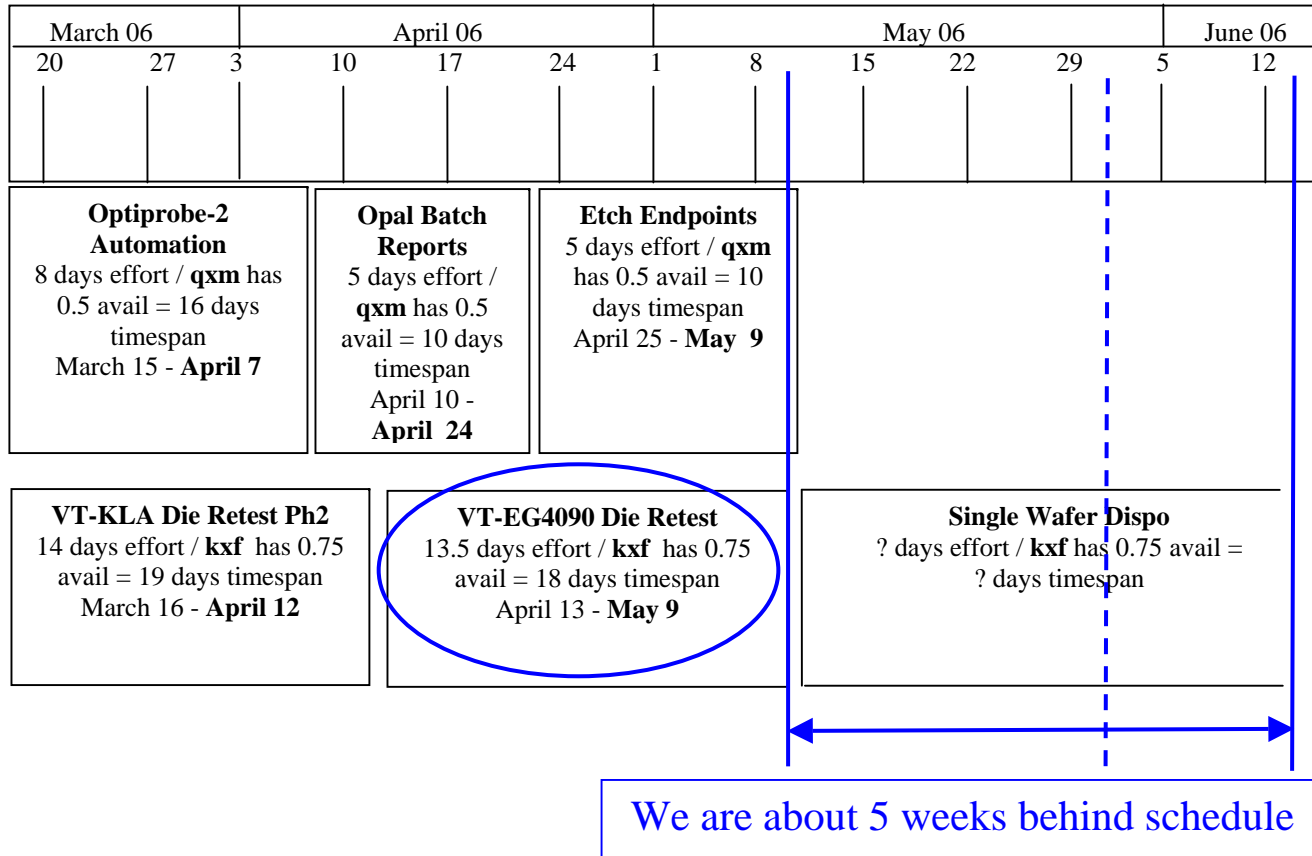
01-02824 Fab2 Versatest V210X with EG4080 Operation Procedure

- Is in signoff under ECN 463329
- The sections on die retest is a duplicate of
01-02682 Fab2 Versatest V210X Operations Procedure
- No new training, certification, etc. updates are needed.



Schedule Status

(original schedule from memo KXF-162)



VT-EG Software Release Schedule

What	Who	OS	CS	Notes
Hold PCR3	KXF	5/08/06	5/31/06	DONE
Retrofit first VT-EG	KXF		6/01/06	We will know which wafers went through the retrofitted software
Retrofit second VT-EG	KXF		6/05/07	If no significant issues with first VT-EG
Retrofit third VT-EG			6/08/07	If no significant issues with first and second VT-EGs
Hold PCR4, review any issues	KXF		6/14/06	Might just issue a memo for approval if no issues and nothing to discuss
Retrofit remaining 5 VT-EG tools	KXF	5/10/06	6/16/06	Assumes no significant issues and no need to run another set of correlation maps to qualify software changes



Signoff Sheet

Yield Engineering Manager	BYB	_____
Test Engineer Manager	BYB	_____
Sort Production Manager	PJX	_____
QA Manager	LHK (for BCK)	_____

Signoff handled through memo system approvals