Outline

Date: 12/06/05
Re: Die Retest Project
To: Memo Log
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File#: KXF-
Category:

CC: <Distributed Electronically>

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Executive Summary

What this is:

A rewrite of two of the executable programs which run on the VT2102 testers (with KLA probers) to add "die retest" functionality similar to that implemented at CMI.

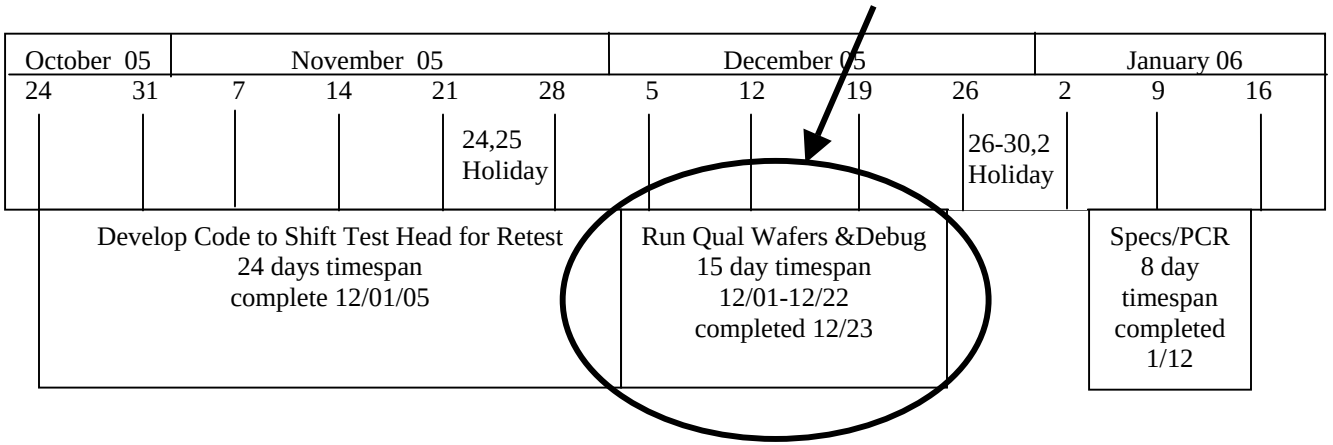
Summary Status:

As per 18Oct meeting (memo kxf-143): CMI's die retest approach (i.e. retesting with another site, CMI plan file entries) has been implemented, and tested on VT-27 (horizontal and sloped quad probe cards, devices 6370 and 29000) and VT-11 (horizontal probe card, device 6370).

Purpose of this Meeting:

To stay on schedule, we want approval to start running 200 qualification wafers in limited production (this means we do NOT rsc these wafers and we do NOT re-run these wafers under the previous software).

According to the schedule (memo KXF-144, CTI VT2100 Die Retest Phase 2 (21Oct05 Plan)), we need to run 200 wafers for qualification:



Changes to the 21Oct05 (memo kxf-144) plan:

Start:	10/24/05	
Ready for Die Retest Qualification Runs (+24 days):	12/01/05	200 wafer qualification
Run Qual Wafers, Debug , Train (+15 days):	12/23/05	
Spec, PCR3 completed, ready for turn-on (+8 days):	**01/12/06**	

21Oct05 Plan: Starting 01Dec05:

week1: 33 wafers on 1 tester
week2: 67 wafers over 2 testers
week3: 100 wafers over 3 testers
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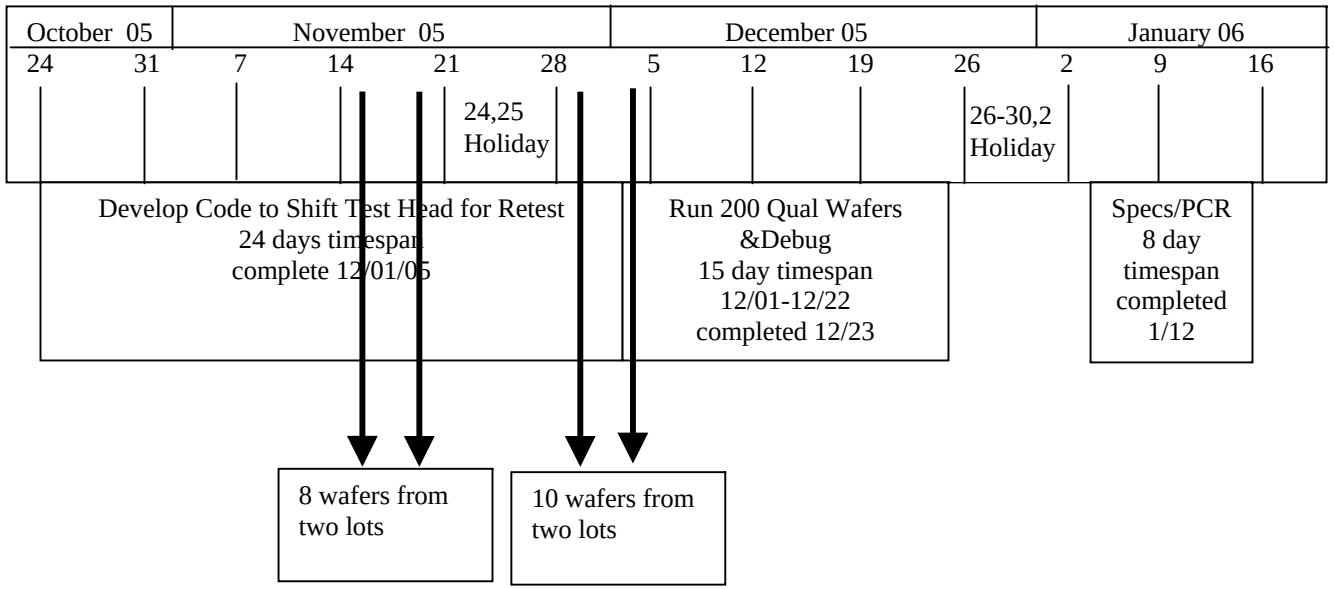
200 wafer qualification

- We were ready to start our 200 wafer qual & debug run on 16Nov05.
  - The schedule put this at 01Dec05
- In 17Nov review meeting (see memo kxf-146), CSD requested that we first run limited wafers across all our probe card configurations in order to:
  a) Debug the code, b) Get a feel for the retest bin settings, runtime increases, and yield improvements.

Run Rate for RSC'd Wafers:



Question:

Will we make our dates if we continue to run qual wafers under RSC?

Limited Wafers Across all Probe Card Configurations - Summary of Results

	Probe Card Device	Test Pgm	Lot Wafers Date	Average Retest Yield	Average Extra Runtime per Wafer
1	Horizontal Quad (vt27) **6370** ~3 sec per head touchdown ~3 sec extra per retest	eng/ft16c370.kxf RE_TEST 3 1 1000 RE_TEST 4 1 1000 RE_TEST 5 1 1000	2540725 wafers 8-13 16Nov05	0.67%	75 seconds
2	Neg Sloped Quad (vt27) **29000** ~10.5 sec per head touchdown ~20 sec extra per retest	eng/f129000a.kxf RE_TEST 3 1 1000 RE_TEST 7 1 1000 RE_TEST 8 1 1000 RE_TEST 10 1 1000 RE_TEST 11 1 1000 RE_TEST 12 1 1000 RE_TEST 13 1 1000	2535074 Wafers 1,3,5 18Nov05 2542075 Wafers 2,3,4 29Nov05	2.0%	37 minutes
3	Horizontal Dual (vt11) **6370** ~3 sec per head touchdown ~3 sec extra per retest	eng/dt16c370.kxf RE_TEST 3 1 1000 RE_TEST 4 1 1000 RE_TEST 5 1 1000	2543213a Wafers 3,5,6 02Dec05	0%	23 seconds

These rsc'd wafers turned out to be high yielding. The next tester over had a lot that would have been much better to run.

Due to the rsc'ing requirement, we could not switch lots on the fly in order to get better yield recovery data

What is Needed to Meet the Schedule: In order to speed things up, can we:

- NOT reprobe the wafers run under the new software for 6370 (at the least)?
- NOT rsc 6370 wafers to run under the new software?

Note that we have to do two types of testing simultaneouly:

- Run 200 qual wafers, figure out which bins to setup for retesting in plan file
- Software alpha and beta testing (for operator usability)

Plan:

- In the beginning we will run the new software for production ***during days, when KXF is around*** to respond to questions and bugs (i.e., software "alpha" testing).

- When a some subset of operators across all shifts are comfortable with the new software we will move into software "beta" (i.e., kxf is not there) testing

Approvals

Approvals will be via the memo system, for the people decided upon at this meeting.

Appendix

Payback Summary Details

	Probe Card Device	Test Pgm	Lot Date	Wafer Results	Notes
1	Horizontal Quad vt27 **6370** ~3 sec per head touchdown ~3 sec extra per retest	eng/ft16c370.kxf RE_TEST 3 1 1000 RE_TEST 4 1 1000 RE_TEST 5 1 1000	2540725 16Nov05	Wafer 8: 57 min runtime, 2543 yield, 24 retests, 21 retests got changes, 21 die recovered / 2543=**0.8%** Wafer 9: 43 min runtime, 2339 yield, 27 retests, 14 retests got changes, 14 die recovered /2339=**0.6%** Wafer 10: 45 min runtime, 2544 yield, 25 retests, 17 retests got changes, 17 die recovered / 2544= **0.7%** Wafer 11: 44 min runtime, 2530 yield, 27 retests, 19 retests got changes, 18 die recovered / 2530 = **0.7%** Wafer 12: 43 min runtime, 2508 yield, 21 retests, 9 retests got changes, 9 die recovered / 2508 = **0.4%** Wafer 13: 44 min runtime, 2563 yield, 27 retests, 21 retest got results, 21 die recovered /2563 = **0.8%**	av no of retests = 25 retests x 3 sec extra test time per retest = **75 sec av extra test time per wafer** **av retest yield % = 0.67** Ratio of extra test time to extra yield = 75 / 0.67 = 1.8 min extra test time/per percent yield
2	Neg Sloped Quad vt27 **29000**	eng/f129000a.kxf RE_TEST 3 1 1000 RE_TEST 7 1 1000 RE_TEST 8 1 1000	2535074 18Nov05	Wafer 1: 68 min runtime, 738 yield, 112 retests, 25 retests got changes, 15 die recovered / 738 = **2%**	av no of retests = 111 retests x 20 sec extra test time per retest = 2220 sec av extra test time per wafer =

	Probe Card Device	Test Pgm	Lot Date	Wafer Results	Notes
	~10.5 sec per head touchdown ~20 sec extra per retest	RE_TEST 10 1 1000 RE_TEST 11 1 1000 RE_TEST 12 1 1000 RE_TEST 13 1 1000		Wafer 3: 65 min runtime, 747 yield, 103 retests, 27 retests got changes, 11 die recovered / 747 = **1.5%** Wafer 5: 65 min runtime, 744 yield, 117 retests, 28 retests got changes, 19 die recovered / 744 = **2.5%**	**37 min av extra test time per wafer** **av retest yield % = 2.0%** Ratio of extra test time to extra yeild = 2220 / 2.0 = 18.5 min extra test time/per percent yield
3	Neg Sloped Quad vt27 **29000** ~10.5 sec per head touchdown ~20 sec extra per retest	eng/f129000a.kxf RE_TEST 7 1 1000 RE_TEST 8 1 1000 RE_TEST 10 1 1000 RE_TEST 11 1 1000 RE_TEST 12 1 1000	2542075 29Nov05	Wafer 1: 81 min runtime, 637 yield, 174 retests, 107 retests got changes, 89 die recovered / 637 = 14.0% Wafer 2: 68 min runtime, 731 yield, 129 retests, 20 retests got changes, 14 die recovered / 731 = **1.9%** Wafer 3: 69 min runtime, 710 yield, 128 retests, 13 retests got changes, 13 die recovered / 710 = **1.8%** Wafer 4: 72 min runtime, 674 yield, 122 retests, 28 retests got changes, 26 die recovered / 674 = **3.9%** Wafer 5: 74 min runtime, 696 yield, 158 retests, 90 retests got changes, 72 die recovered / 696 = 10.3%	Wafer 4 map looked messed up Are Wafer 1 and 5 outliers? Wafer 2,3 stats are consistent with previous 29000 run.
	Horizontal Dual vt11 **6370**	eng/dt16c370.kxf RE_TEST 3 1 1000 RE_TEST 4 1 1000 RE_TEST 5 1 1000	2543213a 02Dec05	Wafer 3: 79 min runtime, 2468 yield, 12 retests, 0 retests got changes Wafer 5: 80 min runtime, 2529 yield, 7 retests, 0 retests got changes Wafer 6: 81 min runtime, 2513 yield, 4 retests, 0 retests got changes	Also ran Wafers 1 & 2. Found bug at the top of Wafer 2: was no doing die retesting for dual probe card. Fixed bug.
	Neg Sloped Dual	eng/dt153120.kxf			retest bins are per brt 30Nov05

	Probe Card Device	Test Pgm	Lot Date	Wafer Results	Notes
	7C53120CT	RE_TEST 5 1 1000 RE_TEST 9 1 1000 RE_TEST 12 1 1000			
	Pos Sloped Dual 6341	eng/dt16c341.kxf RE_TEST 3 1 1000 RE_TEST 4 1 1000 RE_TEST 5 1 1000			same retest bins as 6370
	Pos Sloped Dual 6602	eng/dt16c602.kxf RE_TEST 3 1 1000 RE_TEST 4 1 1000 RE_TEST 5 1 1000			same retest bins as 6370